UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,812	07/30/2001	Frank C. Hoppensteadt	9138-0018	9742

7590 02/26/2004

Thomas D MacBlain
Gallagher & Kennedy
2575 East Camelback Road
Phoenix, AZ 85016

EXAMINER	
HOLMES, MICHAEL B	

ART UNIT	PAPER NUMBER
2121	6

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,812	HOPPENSTEADT ET AL.	
	Examiner	Art Unit	
	Michael B. Holmes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *(3)* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-4,13 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-12 and 15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. Box 1450, Alexandria, Virginia 22313-1450 – WWW.USPTO.GOV

Examiner's Detailed Office Action

1. This action is responsive to application **09/831,812,** filed **July 30, 2000**.

2. **Claims 1-4** and **13-14** have been canceled without prejudice.

3. **Claim 6, 7,** and **25** have been amended.

4. **Claims 5-12** and **15-25** remain and have been examined.

Information Disclosure Statement

5. Applicant is respectfully remind of the Duty to disclose 37 C.F.R. 1.56 all pertinent information and material pertaining to the patentability of applicant's claimed invention, by continuing to submitting in a timely manner PTO-1449, Information Disclosure Statement (IDS) with the filing of applicant's of application or thereafter.

Drawings

6. The formal drawings have been reviewed by the United States Patent & Trademark Office of Draftperson's Patent Drawings Review. PTO-Form 948 has been provided.

Specification

7. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is required in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Interpretation

8. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow. . . . The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed. . . . An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process."). *see* MPEP § 2106

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> **(b) the invention was patented** or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claims 5-10, 11-12, 15-18** are rejected under 35 U.S.C. 102(b) as being anticipated by **Woodall (USPN 5,446,828), Filed: March 18, 1993; Date of patent: August 29, 1992.**

Regarding claim 5:

Woodall teaches,

A neurocomputer comprising:

a plurality of n oscillating processing elements; **[Abstract; ("***A nonlinear oscillator (10) includes a neural network (12) having at least one output (12a) for outputting a one dimensional vector. The neural network includes a plurality of layers, including an input layer, an output layer, and at least one hidden layer. Each of the layers includes at least one* ***processing element*** *(PE) that is interconnected to processing elements of adjacent layers.***")]**

a plurality of no more than n connectors, each of said connectors being operably coupled with a corresponding one of said elements; **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention. The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase,* ***and then directed to respective taps of the m delay lines 14', from where the***

adjusted elements are fed back into the neural network 12. *The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.*")]

a conductive medium operably coupled with said connectors; **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention. The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector.* ***The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector.*** *The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.*")] and

a rhythmic input operably coupled with said medium. **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention. The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13.* ***In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines***

14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.")]

Regarding claim 6:

Woodall teaches,

A neurocomputer comprising:

a plurality of n processing element means; **[col. 2, line 4-18 ("***FIG. 1c illustrates in greater detail an exemplary embodiment of the neural network 12, also referred to herein as a primary neural network. The neural network 12 is comprised of four layers designated as layer 0, the output layer; layer 1, the second hidden layer; layer 2, the first hidden layer; and layer 4, the input layer. Layer 0 has one neuron, or linear* ***processing element (PE1)****, layer 1 has three PEs (PE1-PE3), layer 2 has eight PEs (PE1-PE8) and layer 4 has 12 PEs, illustrated in FIG. 1c as delay line stages -1 to -12. A specific PE is identified first by the layer in which it resides, and then by the PE number. For example, PE2 of the second hidden layer is designated as (1, PE2) or more simply (1, 2).*")]

a plurality of no more than n connectors operably coupled with said element means, means for simultaneously applying an oscillatory signal to each of said element means via said connectors;

[col. 2, line 4-18 ("*FIG. 1c illustrates in greater detail an exemplary embodiment of the neural network 12, also referred to herein as a primary neural network. The neural network 12 is comprised of four layers designated as layer 0, the output layer; layer 1, the second hidden layer; layer 2, the first hidden layer; and layer 4, the input layer.* ***Layer 0 has one neuron, or linear processing element (PE1), layer 1 has three PEs*** *(PE1-PE3),* ***layer 2 has eight PEs*** *(PE1-PE8)* ***and layer 4 has 12 PEs, illustrated in FIG. 1c as delay line stages -1 to -12.*** *A specific PE is identified first by the layer in which it resides, and then by the PE number. For example, PE2 of the second hidden layer is designated as (1, PE2) or more simply (1, 2).*")]

and

means for generating said oscillatory signal operably coupled with signal means for applying.

[(col. 3, line 27-48 "*FIG. 1b illustrates in greater detail an exemplary embodiment of the oscillator 10 of FIG. 1a, and shows a feedback gain/phase control circuit 16 for adjusting the feedback from the output 12a to a desired level and/or phase (polarity) at a selected input to the delay line 14. The modified output vector 12b from the gain/phase control circuit 16 may be applied to any one of the delay line 14 taps, as indicated by the switching function (SW).* ***In the oscillator 10, the dimensionality of the output data is a function of the neural network dimensionality****. The generalized nonlinear neural network oscillator 10 enables a complex order of neural network 12 outputs, delay line 14 outputs (historical values), and external inputs (forcing functions) to be manipulated into a single or a multidimensional vector, and then be placed into the neural network 12 input. The delay line 14 shifts single or multidimensional vector sets. The gain/phase feedback circuit 16 may be a linear circuit, a nonlinear circuit, or another neural network. Also, neural network paradigms that include distributed delays through*

the neural networks may be used in the nonlinear neural network oscillator 10.")]

Regarding claim 7:

Woodall teaches,

The neurocomputer of claim 6, wherein:

each of said connectors is operably coupled with a corresponding one of said element means.

[(col. 3, line 27-48 "*FIG. 1b illustrates in greater detail an exemplary embodiment of the oscillator 10 of FIG. 1a, and shows a feedback gain/phase control circuit 16 for adjusting the feedback from the output 12a to a desired level and/or phase (polarity) at a selected input to the delay line 14. The modified output vector 12b from the gain/phase control circuit 16 may be applied to any one of the delay line 14 taps, as indicated by the switching function (SW). In the oscillator 10, the dimensionality of the output data is a function of the neural network dimensionality.* ***The generalized nonlinear neural network oscillator 10 enables a complex order of neural network 12 outputs****, delay line 14 outputs (historical values), and external inputs (forcing functions) to be manipulated into a single or a multidimensional vector, and* ***then be placed into the neural network 12 input****. The delay line 14 shifts single or multidimensional vector sets. The gain/phase feedback circuit 16 may be a linear circuit, a nonlinear circuit, or another neural network. Also, neural network paradigms that include distributed delays through the neural networks may be used in the nonlinear neural network oscillator 10.*")]

Regarding claim 8:

Woodall teaches,

The neurocomputer of claim 6, wherein:

said element means comprise oscillators. **[Abstract ("***A* ***nonlinear oscillator*** *(10) includes a neural network (12) having at least one output (12a)* ***for*** *outputting a one dimensional vector. The nonlinear oscillator further includes a feedback network (16) that is interposed between the output of the neural network and the input of the input layer for modifying a magnitude and/or a polarity of the one dimensional output vector prior to the sample of the one dimensional output vector being applied to the input of the analog delay line.")]*

Regarding claim 9:

Woodall teaches,

The neurocomputer of claim 6, wherein:

said means for applying comprises a conductive medium. **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention.* ***The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The***

***control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.*")]**

Regarding claim 10:

Woodall teaches,

The neurocomputer of claim 6, wherein:

said means for generating comprises a rhythmic input. **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention. The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12.* ***The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.*")]**

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. **Claims 11-12** and **15-18** are rejected under 35 U.S.C. 102(b) as being anticipated by **Burger (USPN 4,815,475), Filed: June 2, 1987; Date of patent: March 28, 1989**.

Regarding claim 11:

Burger teaches,

An oscillatory neurocomputer comprising:

a number n of oscillating elements, **[(col. 2, line 56-68 "***The modulation system comprises, in combination:* ***a first variable frequency oscillator, a second variable frequency oscillator****, a first adjustment means, a second adjustment means, a gating means, and a stimulation means. The first variable frequency oscillator has an output. The output of the first variable frequency oscillator is a first pulsed waveform which has a first pulsed waveform frequency. The second variable frequency oscillator has an output. The output of the second variable frequency oscillator is a second pulsed waveform which has a second pulsed waveform frequency. The first pulsed waveform frequency is greater than the second pulsed waveform frequency.***")]** a source of a rhythmic forcing input, **[(col. 5, line 59 to col. 6, line 4 "***FIGS. 1 and 2 each employ similar numbers to indicate similar elements. FIG. 1 depicts a preferred embodiment of the present invention. The modulation system for evoked response stimulation is shown in FIG. 1*

comprises gating means 26, such as a (N)AND gate, for effecting a logical operator AND. Gating means 26 is used to gate the interaction of ***first variable frequency oscillator 24, such as a Signetics SE566 function generator*** *with the inputs from: (a) manual safety and control switch 50, such as a single pole single throw momentary contact normally open switch, which is shown in FIG. 1 operably connected to inverter 51 which is operably connected to third input 87 of gating means 26.*")]

a medium interconnecting the source of rhythmic forcing input to each oscillating element, each oscillating element having an oscillating frequency, **[(col. 5, line 59 to col. 6, line 4 "***FIGS. 1 and 2 each employ similar numbers to indicate similar elements. FIG. 1 depicts a preferred embodiment of the present invention.* ***The modulation system for evoked response stimulation is shown in FIG. 1 comprises gating means 26, such as a (N)AND gate, for effecting a logical operator AND. Gating means 26 is used to gate the interaction of first variable frequency oscillator 24, such as a Signetics SE566 function generator*** *with the inputs from: (a) manual safety and control switch 50, such as a single pole single throw momentary contact normally open switch, which is shown in FIG. 1 operably connected to inverter 51 which is operably connected to third input 87 of gating means 26.*")]

the oscillating frequency fl of at least one of the oscillating elements differing from the oscillating frequency f2 of at least one other of the oscillating elements, **[(col. 2, line 56-68 "***The modulation system comprises, in combination:* ***a first variable frequency oscillator, a second variable frequency oscillator****, a first adjustment means, a second adjustment means, a gating means, and a stimulation means. The first variable frequency oscillator has an output. The output of the first variable frequency oscillator is a first pulsed waveform which has a first*

pulsed waveform frequency. The second variable frequency oscillator has an output. The output of the second variable frequency oscillator is a second pulsed waveform which has a second pulsed waveform frequency. ***The first pulsed waveform frequency is greater than the second pulsed waveform frequency.***")]

the source of a rhythmic forcing input producing an input of a third frequency f3, **[FIG. 2; (col. 4, line 44-51** "*FIG. 2 is a schematic block diagram of how this invention may be setup to allow for microprocessor control over each stimulation source and how an external sensor may be interfaced and used to alter control settings in place of a human operator. In this embodiment signal amplitude as well as pulse repetition rate is accomplished within the physical limits of each transducer.*")]

establishing communication between the at least one oscillating element and the at least one other oscillating element. **[ABSTRACT** ("*A modulation system used for non-surgical biomedical stimulation and for research in the area of evoked responses and a method thereof is described.* ***The modulation system comprises an AND gate used to gate the interaction of a variable frequency oscillator with the inputs from a manual safety and control switch connected to an inverter which is connected to a third input of the AND gate.***")]

Regarding claim 12:

Burger teaches,

An oscillatory neurocomputer according to claim 11, wherein f3 is substantially the difference between f1 and f2. **[(col. 6, line 28-48** ***"Gating means 26 has an output 90 operably connected to input 91 of pulse width modulating means 27****, such as a pulse width monostable oscillator, oralternatively output 90 can be operably connected directly to input 30 of the stimulation means. Gating means 26 may also be controlled in response to an output from an evoked response sensing means as received by an interfacing means and computed by a processor means.* ***Output 90 of gating means 26 has a composite waveform 75 which is a composite of first pulsed waveform 37 and second pulsed waveform 38****. As shown in FIG. 1, waveform 75 is further conditioned by pulse width modulating means 27 generating a final waveform 40 at output 28 of pulse width modulating means 27. Pulse width modulating means 27 has a pulse width waveform 39. The final width of final waveform 40 is established either by an operator who varies and controls pulse width modulating means by employing control input 23, such as a variable resistor, or, as shown in FIG. 2, by an evoked response sensing means which can vary and control pulse width modulating means 27."***)]

Regarding claim 15:

Burger teaches,

An oscillatory neurocomputer according to claim 11, wherein the oscillating elements are electronic oscillators, **[(col. 5, line 59 to col. 6, line 4** *"FIGS. 1 and 2 each employ similar numbers to indicate similar elements. FIG. 1 depicts a preferred embodiment of the present*

invention. ***The modulation system for evoked response stimulation is shown in FIG. 1 comprises gating means 26, such as a (N)AND gate, for effecting a logical operator AND. Gating means 26 is used to gate the interaction of first variable frequency oscillator 24, such as a Signetics SE566 function generator*** *with the inputs from: (a) manual safety and control switch 50, such as a single pole single throw momentary contact normally open switch, which is shown in FIG. 1 operably connected to inverter 51 which is operably connected to third input 87 of gating means 26.*")]

the source of a rhythmic forcing input is a function generator and the interconnecting medium is an electrically conductive medium electrically connecting the source of a rhythmic forcing input to the oscillators. **[(col. 5, line 59 to col. 6, line 4** "*FIGS. 1 and 2 each employ similar numbers to indicate similar elements. FIG. 1 depicts a preferred embodiment of the present invention.* ***The modulation system for evoked response stimulation is shown in FIG. 1 comprises gating means 26, such as a (N)AND gate, for effecting a logical operator AND. Gating means 26 is used to gate the interaction of first variable frequency oscillator 24, such as a Signetics SE566 function generator*** *with the inputs from: (a) manual safety and control switch 50, such as a single pole single throw momentary contact normally open switch, which is shown in FIG. 1 operably connected to inverter 51 which is operably connected to third input 87 of gating means 26.*")]

Regarding claim 16:

Burger teaches,

An oscillatory neurocomputer according to claim 15, wherein the function generator provides a forcing signal having a carrier frequency and information content modulating the carrier frequency, **[(col. 5, line 59 to col. 6, line 4 "***FIGS. 1 and 2 each employ similar numbers to indicate similar elements. FIG. 1 depicts a preferred embodiment of the present invention.* ***The modulation system for evoked response stimulation is shown in FIG. 1 comprises gating means 26, such as a (N)AND gate, for effecting a logical operator AND. Gating means 26 is used to gate the interaction of first variable frequency oscillator 24, such as a Signetics SE566 function generator*** *with the inputs from: (a) manual safety and control switch 50, such as a single pole single throw momentary contact normally open switch, which is shown in FIG. 1 operably connected to inverter 51 which is operably connected to third input 87 of gating means 26.*"**)]**

the oscillators responding to the impression of the forcing signal onto the conductive medium to produce information content modulation substantially the same as that of the conductive medium. **[FIG. 2; (col. 4, line 44-51 "***FIG. 2 is a schematic block diagram of how this invention may be setup to allow for microprocessor control over each stimulation source and how an external sensor may be interfaced and used to alter control settings in place of a human operator. In this embodiment signal amplitude as well as pulse repetition rate is accomplished within the physical limits of each transducer.*"**)]**

Regarding claim 17:

Burger teaches,

An oscillatory neurocomputer according to claim 11, wherein the number n of oscillating elements is greater than two, **[FIG. 1,** item **24, 25, 90, 27 (col. 4, line 40-41** "*FIG. 1 is a schematic block diagram of diagram of the simplest embodiment of the invention.*"**)]**

a first subset of the oscillating elements communicate at a frequency f3 of rhythmic forcing input from the source, **[(col. 6, line 28-48** "*Gating means 26 has an output 90 operably connected to input 91 of pulse width modulating means 27, such as a pulse width monostable oscillator, oralternatively output 90 can be operably connected directly to input 30 of the stimulation means. Gating means 26 may also be controlled in response to an output from an evoked response sensing means as received by an interfacing means and computed by a processor means.* ***Output 90 of gating means 26 has a composite waveform 75 which is a composite of first pulsed waveform 37 and second pulsed waveform 38****. As shown in FIG. 1, waveform 75 is further conditioned by pulse width modulating means 27 generating a final waveform 40 at output 28 of pulse width modulating means 27. Pulse width modulating means 27 has a pulse width waveform 39. The final width of final waveform 40 is established either by an operator who varies and controls pulse width modulating means by employing control input 23, such as a variable resistor, or, as shown in FIG. 2, by an evoked response sensing means which can vary and control pulse width modulating means 27.*"**)]** and

at least one second subset of the oscillating elements communicate at least one further frequency

f4 of rhythmic forcing input from the source. **[(col. 6, line 28-48** *"Gating means 26 has an output 90 operably connected to input 91 of pulse width modulating means 27, such as a pulse width monostable oscillator, or alternatively output 90 can be operably connected directly to input 30 of the stimulation means. Gating means 26 may also be controlled in response to an output from an evoked response sensing means as received by an interfacing means and computed by a processor means. Output 90 of gating means 26 has a composite waveform 75 which is a composite of first pulsed waveform 37 and second pulsed waveform 38.* ***As shown in FIG. 1, waveform 75 is further conditioned by pulse width modulating means 27 generating a final waveform 40 at output 28 of pulse width modulating means 27. Pulse width modulating means 27 has a pulse width waveform 39.*** *The final width of final waveform 40 is established either by an operator who varies and controls pulse width modulating means by employing control input 23, such as a variable resistor, or, as shown in FIG. 2, by an evoked response sensing means which can vary and control pulse width modulating means 27."***)]**

Regarding claim 18:

Burger teaches,

An oscillatory neurocomputer according to claim 15, wherein content varying one oscillator from its oscillating frequency is communicated to and varies from its oscillating frequency another oscillator in communication with the one oscillator. **[FIG. 2; (col. 4, line 44-51** *"FIG. 2 is a schematic block diagram of how this invention may be setup to allow for microprocessor control over each stimulation source and how an external sensor may be interfaced and used to*

alter control settings in place of a human operator. In this embodiment signal amplitude as well as pulse repetition rate is accomplished within the physical limits of each transducer.")]

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> **(b) the invention was patented** or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. **Claims 19-25** are rejected under 35 U.S.C. 102(b) as being anticipated by **Woodall (USPN 5,446,828), Filed: March 18, 1993; Date of patent: August 29, 1992.**

Regarding claim 19:

Woodall teaches,

A neurocomputer including:

(a) an array of oscillators, at least a plurality of said oscillators having differing frequencies,

**[(col. 3, line 27-48 "*FIG. 1b illustrates in greater detail an exemplary embodiment of the oscillator 10 of FIG. 1a, and shows a feedback gain/phase control circuit 16 for adjusting the feedback from the output 12a to a desired level and/or phase (polarity) at a selected input to the delay line 14. The modified output vector 12b from the gain/phase control circuit 16 may be applied to any one of the delay line 14 taps, as indicated by the switching function (SW). In the oscillator 10, the dimensionality of the output data is a function of the neural network*

dimensionality. The generalized nonlinear neural network oscillator 10 enables a complex order of neural network 12 outputs, delay line 14 outputs (historical values), and external inputs (forcing functions) to be manipulated into a single or a multidimensional vector, and then be placed into the neural network 12 input. The delay line 14 shifts single or multidimensional vector sets. The gain/phase feedback circuit 16 may be a linear circuit, a nonlinear circuit, or another neural network. Also, neural network paradigms that include distributed delays through the neural networks may be used in the nonlinear neural network oscillator 10.")]

(b) a common conducting medium connected to each of the plurality of oscillators,

[(**col. 3, line 27-48 "*FIG. 1b illustrates in greater detail an exemplary embodiment of the oscillator 10 of FIG. 1a, and shows a feedback gain/phase control circuit 16 for adjusting the feedback from the output 12a to a desired level and/or phase (polarity) at a selected input to the delay line 14. The modified output vector 12b from the gain/phase control circuit 16 may be applied to any one of the delay line 14 taps, as indicated by the switching function (SW).* In the oscillator 10, the dimensionality of the output data is a function of the neural network dimensionality. The generalized nonlinear neural network oscillator 10 enables a complex order of neural network 12 outputs, delay line 14 outputs (historical values), and external inputs (forcing functions) to be manipulated into a single or a multidimensional vector, and then be placed into the neural network 12 input. The delay line 14 shifts single or multidimensional vector sets. The gain/phase feedback circuit 16 may be a linear circuit, a nonlinear circuit, or another neural network. Also, neural network paradigms that include distributed delays through the neural networks may be used in the nonlinear neural network oscillator 10.*")]

(c) a source connected to the conducting medium to impart oscillator signals of various

frequencies to the conducting medium, the signals of various frequencies including frequencies effective to bring two or more of the oscillators into communication. **[(col. 3, line 27-48 "*FIG. 1b illustrates in greater detail an exemplary embodiment of the oscillator 10 of FIG. 1a, and shows a feedback gain/phase control circuit 16 for adjusting the feedback from the output 12a to a desired level and/or phase (polarity) at a selected input to the delay line 14. The modified output vector 12b from the gain/phase control circuit 16 may be applied to any one of the delay line 14 taps, as indicated by the switching function (SW).* In the oscillator 10, the dimensionality of the output data is a function of the neural network dimensionality. The generalized nonlinear neural network oscillator 10 enables a complex order of neural network 12 outputs, delay line 14 outputs (historical values), and external inputs (forcing functions) to be manipulated into a single or a multidimensional vector, and then be placed into the neural network 12 input. The delay line 14 shifts single or multidimensional vector sets. The gain/phase feedback circuit 16 may be a linear circuit, a nonlinear circuit, or another neural network. Also, neural network paradigms that include distributed delays through the neural networks may be used in the nonlinear neural network oscillator 10.*")]

Regarding claim 20:

Woodall teaches,

An oscillatory neurocomputer according to claim 19, wherein the oscillators include feedback circuits connected with the medium. **[(Abstract ("*The nonlinear oscillator further includes a feedback network (16) that is interposed between the output of the neural network and the*

input of the input layer for modifying a magnitude and/or a polarity of the one dimensional output vector prior to the sample of the one dimensional output vector being applied to the input of the analog delay line. The analog delay line is capable of being shifted in either a first or a second direction. *Connection weights of the neural network are trained on a deterministic sequence of data from a chaotic source or may be a representation of a stochastic process, wherein each of the weights is randomly selected"*)]

Regarding claim 21:

Woodall teaches,

An oscillatory neurocomputer according to claim 20, wherein the oscillators are phase locked loops. **[(col. 3, line 27-48 "***FIG. 1b illustrates in greater detail an exemplary embodiment of the oscillator 10 of FIG. 1a, and* ***shows a feedback gain/phase control circuit 16 for adjusting the feedback from the output 12a to a desired level and/or phase (polarity) at a selected input to the delay line 14. The modified output vector 12b from the gain/phase control circuit 16 may be applied to any one of the delay line 14 taps, as indicated by the switching function (SW).*** *In the oscillator 10, the dimensionality of the output data is a function of the neural network dimensionality. The generalized nonlinear neural network oscillator 10 enables a complex order of neural network 12 outputs, delay line 14 outputs (historical values), and external inputs (forcing functions) to be manipulated into a single or a multidimensional vector, and then be placed into the neural network 12 input. The delay line 14 shifts single or multidimensional vector sets. The gain/phase feedback circuit 16 may be a linear circuit, a nonlinear circuit, or another neural network. Also, neural network paradigms that include distributed delays through*

the neural networks may be used in the nonlinear neural network oscillator 10. **")]IEEE** note: A phase locked loop ("PLL") is a circuit for synchronizing a local variable or rate controlled oscillator with the phase of a transmitted signal i.e., widely used in space communications for coherent carrier tracking, and threshold extension, bit synchronization and symbol synchronization. IEEE 100, Seventh Ed.

Regarding claim 22:

Woodall teaches,

A method of enabling communication of a characteristic between a first processing element oscillating at a first frequency and a second processing element oscillating at a second frequency different from the first frequency, the method comprising the steps of:

operably coupling the first element to a medium; **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention.* ***The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals."***)]

operably coupling the second element to said medium; **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention.* ***The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.")]***

operably coupling said medium to a rhythmic input; **[(col. 3, line 49-65 "***FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention.* ***The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.")]** and

causing said rhythmic input to oscillate said medium at a third frequency. **[(col. 3, line 49-65** "*FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention.* ***The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.***")]

Regarding claim 23:

Woodall teaches,

The method of claim 22, wherein:

said third frequency comprises a frequency substantially equal to the difference between the first frequency and the second frequency. **[FIG. 2r; (col. 8, line 37-44** "*FIG. 2r: This figure shows a relatively large variation in the output 12a for two closely similar input vectors (V1 and V2). For this example, V1 is -9, 3, 6, -1, 7 and V2 is -9, 3, 1, -1, 7. The neural network 12 was seeded with the random weights of Appendix B, and the delay line 14 is driven with the input vectors by the external forcing function.*) **& (col. 8, line 54-57** "*As was shown in FIG. 2r, the nonlinear neural network oscillator can be used as a vector converter to produce large vectoral differences for*

input vectors that have small linear differences.")]

Regarding claim 24:

Woodall teaches,

A method of enabling communication of a characteristic between a plurality of n oscillating processing elements comprising the steps of:

operably coupling each of the plurality of n elements to a corresponding one of a plurality of no more than n connectors; **[col. 2, line 4-18 ("***FIG. 1c illustrates in greater detail an exemplary embodiment of the neural network 12, also referred to herein as a primary neural network. The neural network 12 is comprised of four layers designated as layer 0, the output layer; layer 1, the second hidden layer; layer 2, the first hidden layer; and layer 4, the input layer.* ***Layer 0 has one neuron, or linear processing element (PE1), layer 1 has three PEs*** *(PE1-PE3),* ***layer 2 has eight PEs*** *(PE1-PE8)* ***and layer 4 has 12 PEs, illustrated in FIG. 1c as delay line stages -1 to -12.*** *A specific PE is identified first by the layer in which it resides, and then by the PE number. For example, PE2 of the second hidden layer is designated as (1, PE2) or more simply (1, 2).")]*

operably coupling each one of said connectors to a conductive medium; **[(col. 3, line 49-65** "*FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention. The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13. In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The*

control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. ***The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector.*** *The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.*")] and

operably coupling said medium to a rhythmic input. [**(col. 3, line 49-65** "*FIG. 1d is a block diagram showing a generalized nonlinear neural network oscillator 10 of the invention. The neural network 12 provides a n-dimensional output vector which is fed back to an input of a control block 13.* ***In the control block 13 the elements of the n-dimensional output vector are divided, adjusted in gain and in phase, and then directed to respective taps of the m delay lines 14', from where the adjusted elements are fed back into the neural network 12. The control block 13 also receives a control vector and/or a forcing function for use in modifying the elements of the output vector. The control block 13 may apply forcing function data to the neural network 12 with or without feedback from the n-dimensional output vector. The control block 13 may incorporate a neural network to combine or divide vector elements into common feedback signals.***")]

Regarding claim 25:

Woodall teaches,

In a neurocomputer, a number n of active elements and a medium having no more than n connections operably coupled to each of the active elements for application of an input signal thereto, said active elements being phase locked loop oscillators. [**(col. 3, line 27-48** "*FIG. 1b*

illustrates in greater detail an exemplary embodiment of the oscillator 10 of FIG. 1a, and ***shows a feedback gain/phase control circuit 16 for adjusting the feedback from the output 12a to a desired level and/or phase (polarity) at a selected input to the delay line 14. The modified output vector 12b from the gain/phase control circuit 16 may be applied to any one of the delay line 14 taps, as indicated by the switching function (SW).*** *In the oscillator 10, the dimensionality of the output data is a function of the neural network dimensionality. The generalized nonlinear neural network oscillator 10 enables a complex order of neural network 12 outputs, delay line 14 outputs (historical values), and external inputs (forcing functions) to be manipulated into a single or a multidimensional vector, and then be placed into the neural network 12 input. The delay line 14 shifts single or multidimensional vector sets. The gain/phase feedback circuit 16 may be a linear circuit, a nonlinear circuit, or another neural network. Also, neural network paradigms that include distributed delays through the neural networks may be used in the nonlinear neural network oscillator 10.* **")] IEEE** note: A phase locked loop ("PLL") is a circuit for synchronizing a local variable or rate controlled oscillator with the phase of a transmitted signal i.e., widely used in space communications for coherent carrier tracking, and threshold extension, bit synchronization and symbol synchronization. IEEE 100, Seventh Ed.

Conclusion

11. The prior art made of record and (listed of form **PTO-892**) not relied upon is considered pertinent to applicant's disclosure as follows. Applicant or applicant's representative is respectfully reminded that in process of patent prosecution i.e., amending of claims in response to a rejection of claims set forth by the Examiner per Title 35 U.S.C. The patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and any objections made. Moreover, applicant or applicant's representative must clearly show how the amendments avoid or overcome such references and objections. *See* **37 CFR § 1.111(c)**.

Correspondence Information

12. Any inquiries concerning this communication or earlier communications from the examiner should be directed to **Michael B. Holmes** who may be reached via telephone at **(703) 308-6280**. The examiner can normally be reached Monday through Friday between 8:00 a.m. and 5:00 p.m. eastern standard time.

If you need to send the Examiner, a facsimile transmission regarding After Final issues, please send it to **(703) 746-7238**. If you need to send an Official facsimile transmission, please send it to **(703) 746-7239**. If you would like to send a Non-Official (draft) facsimile transmission the fax is **(703) 746-7240**. If attempts to reach the examiner by telephone are unsuccessful, the **Examiner's Supervisor, Anil Khatri**, may be reached at **(703) 305-0282**.

Any response to this office action should be mailed too:

Director of Patents and Trademarks Washington, D.C. 20231. Hand-delivered responses should be delivered to the Receptionist, located on the fourth floor of **Crystal Park II, 2121 Crystal Drive Arlington, Virginia.**

Michael B. Holmes
Patent Examiner
Artificial Intelligence
Art Unit 2121
United States Department of Commerce
Patent & Trademark Office